Click here for production status of specific part numbers.

MAX25610A/MAX25610B

Synchronous Buck and Buck-Boost LED Driver/DC-DC Converter

General Description

The MAX25610A/MAX25610B are fully synchronous LED drivers that provide constant output current to drive high-power LEDs. The MAX25610A/MAX25610B integrate two 60mΩ power MOSFETs for synchronous operation, minimizing external components. Flexible configuration supports buck, inverting buck-boost, and boost conversion. The devices incorporate current-mode control that provides fast transient response and eases loop stabilization. The MAX25610A/MAX25610B include cycle by cycle current limiting, output overvoltage protection (OVP), open-string protection, output short-circuit protection (SCP), and thermal shutdown.

In LED driver applications, the MAX25610A/MAX25610B provide analog dimming of the LED current through the REFI pin, and PWM dimming through the PWMDIM pin. Switching is enabled when PWMDIM is high, and disabled with both MOSFETs off when PWMDIM is low. Analog programming of the PWMDIM pin enables the built-in digital dimming function, with dimming frequency selected by the PWMFRQ pin.

The MAX25610A/MAX25610B include two 5V regulators. A regulated 5V between V_{CC} and AGND is used for IC bias, REFI and PWMFRQ programming. Another low current regulated 5V between V_{EE} and INN is used for analog PWMDIM and FLT pullup. Both PWMDIM and FLT reference INN for easy system interface. Switching frequency is internally set at 400kHz for the MAX25610A and 2.2MHz for the MAX25610B. The devices have built-in spread spectrum to reduce EMI noise. External and internal current sense are supported, with ±3% and ±6% respective LED current accuracy.

The MAX25610A/MAX25610B are well-suited for automotive applications requiring high voltage input and can withstand load dump events up to 40V. The devices can also be used as a DC-DC converter using the FB input as feedback for the output voltage divider. The MAX25610A/MAX25610B are available in thermally enhanced 16-pin TSSOP-EP and 16-pin TQFN packages. They are specified to operate over the -40ºC to +125ºC automotive temperature range.

Applications

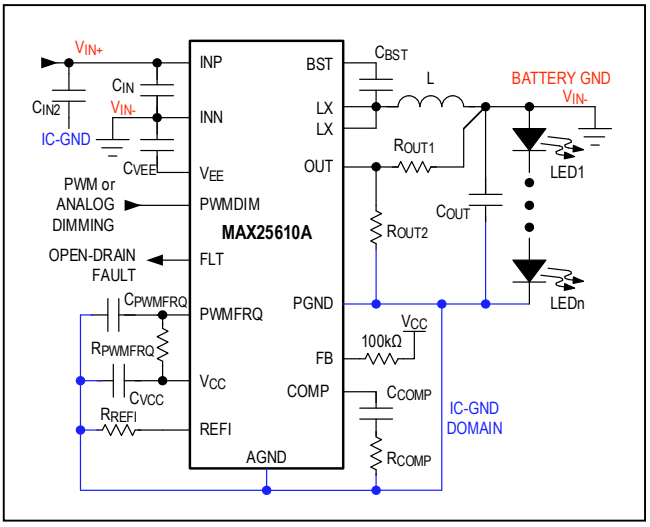
- Automotive Lighting Applications
- Industrial Lighting Applications

Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Integration Minimizes BOM to Save Space and Cost
  - Wide input Voltage Range from 5V to 36V in Buck-Boost LED Driver Applications
  - 2.2MHz Switching Frequency Option Reduces Inductor Size
  - Internal Current-Sense Option Reduces Cost
  - Integrated High and Low-Side Switching MOSFETs
  - PWM Dimming with an Analog Control Voltage Minimizes Additional Components for Dimming
- Wide Dimming Ratio Allows High Contrast Ratio
  - Analog and PWM Dimming
- Multi-Topology Architecture Provides Flexibility
  - Buck LED Driver for 1-to-2 LEDs When Operating of Automotive Battery Applications
  - Inverting Buck-Boost LED Driver for 3-to-5 LEDs When Operating from Automotive Battery Applications
- Protection Features and Wide Temperature Range Increase System Reliability
  - -40°C to +125°C Operating Temperature Range
  - Short-Circuit, Overvoltage, and Thermal Protection
  - $\overline{FLT}$ Flag for Fault Indication

Ordering Information appears at end of data sheet.

Simplified Application Circuit



maxim integrated™

Absolute Maximum Ratings

INP to PGND ..... -0.3V to +40V
INP to LX ..... -0.3V to +40V
LX to PGND ..... -0.3V to +40V
V_{CC} to AGND ..... -0.3V to +6.0V
BST to LX ..... -0.3V to +6.0V
INP to INN ..... -0.3V to +40V
PGND to AGND ..... -0.3V to +0.3V
PWMFRQ, OUT to AGND ..... -0.3V to V_{CC} + 0.3V
REFI, COMP to AGND ..... -0.3V to V_{CC} + 0.3V
FB to AGND ..... -0.3V to +16V
INN to AGND ..... -0.3V to +24V
V_{EE}, PWMDIM to INN ..... -0.3V to +6.0V
$\overline{FLT}$ to INN ..... -0.3V to +6.0V
Short-Circuit Between V_{CC} and AGND ..... Continuous
Continuous Power Dissipation (Multilayer Board) TSSOP-EP (T_A = +70°C, derate 26.1mW/°C above +70°C) 2088mW
Continuous Power Dissipation (Multilayer Board) TQFN-EP (T_A = +70°C, derate 33.3mW/°C above +70°C) 2667mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C
LX Continuous RMS Current (per pin) 1.5A
INP, PGND Continuous RMS Current 2.5A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TSSOP

PACKAGE CODE	U16E+3C
Outline Number	21-0108
Land Pattern Number	90-0120
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	47°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

TQFN

PACKAGE CODE	T1655Y+3C
Outline Number	21-100279
Land Pattern Number	90-0072
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(INP = 12V, INN = AGND = PGND, PWMDIM = INN, Limits are 100% tested at T_A = 25°C and T_A = 125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization from T_A = -40°C to T_A = 125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Input Supply Voltage Range	V_{INP}	t < 1s				40	V
		Buck-boost configuration, PWMDIM = V_{EE}	External digital mode PWM dimming	5		36	
			Internal analog mode PWM dimming	7.5		36	
		Buck configuration		8.3		36	
Quiescent Current	I_{INQ}	PWMDIM = INN V_{INP} = 12V			4	6	mA
		PWMDIM = INN V_{INP} = 36V			5	7	
UV Lockout		Buck mode	Rising threshold	7.5	8	8.3	V
			Falling threshold	7.25	7.75	8.25	
		Buck-boost mode	Rising threshold	4.2	4.45	5	
			Falling threshold	4.1	4.35	4.6	
Switching Current	I_{SW}	MAX25610A	PWMDIM = V_{EE} V_{INP} = 12V		12	20	mA
		MAX25610B	PWMDIM = V_{EE} V_{INP} = 12V		35		
		MAX25610A	PWMDIM = V_{EE} V_{INP} = 33V		20		
V_{CC} REGULATOR							
Output Voltage	V_{CC}	5.5V < V_{INP} < 32V, I_{VCC} = 0mA–20mA		4.89	5.00	5.1	V
Dropout Voltage	V_{CC_DROP}	V_{INP} = 5V, I_{VCC} = 20mA			0.2	0.35	V
Short-Circuit Current Limit	I_{VCC_SC}	V_{CC} shorted to AGND		15	40	100	mA
V_{CC} Current Limit		V_{CC} = 4.8V		30	100	200	mA
V_{EE} REGULATOR							
Output Voltage	V_{EE}	5.5V < V_{INP} < 33V, I_{VEE} = 2mA		4.7	5.00	5.3	V
Dropout Voltage	V_{EE_DROP}	V_{INP} = 5V, I_{VEE} = 3mA			0.1	0.35	V
V_{EE} UVLO Rising	V_{EE_UVLOR}	INP rising		4.1	4.4	4.6	V
V_{EE} UVLO Falling	V_{EE_UVLOF}	INP Falling		4.0	4.25	4.5	V
Short-Circuit Current Limit	I_{VEE_SC}	V_{EE} shorted to INN		10	26	60	mA
INTERNAL MOSFETS							
High-Side MOSFET RDS_{ON}	R_{ON_HS}	I_{LX} = 1A (0.5A per LX pin) (Note 1)			0.06	0.130	Ω
Low-Side MOSFET RDS_{ON}	R_{ON_LS}	I_{LX} = 1A (0.5A per LX pin) (Note 1)			0.06	0.130	Ω
High-Side MOSFET Current Limit Threshold		(Note 2)		3.55	4.25	4.84	A
LX Leakage	$I_{LX,LEAK}$	PWMDIM = INN	V_{INP} = 40V, V_{LX} = 0V or 40V, T_A = +25°C	-5.0		+5.0	µA

Electrical Characteristics (continued)

(INP = 12V, INN = AGND = PGND, PWMDIM = INN, Limits are 100% tested at T_A = 25°C and T_A = 125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization from T_A = -40°C to T_A = 125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL OSCILLATOR							
Switching Frequency	f_{SW}	Dithering off	MAX25610A	370	400	430	kHz
			MAX25610B	2	2.18	2.36	MHz
Minimum On-Time	t_{ON_MIN}	MAX25610A only			100		ns
		MAX25610B only			56	85	
Maximum Duty Cycle	D_{MAX}	MAX25610A only		89	91	94	%
Frequency Dither					+6		%
OVERVOLTAGE							
Overvoltage Threshold Rising	INP_{STOP}	Buck-boost mode	INP rising	33	34.5	36	V
Overvoltage Threshold Falling	INP_{START}	Buck-boost mode	INP falling	32	33.3	34.5	V
PWM DIMMING (PWMDIM)							
Ramp Frequency		Set with external RC on PWMFRQ pin, $f_{DIM} = \frac{3.33 \times 10^{-3}}{R_{PWMFRQ} \times C_{PWMFRQ}}$		200		1000	Hz
PWM Frequency Accuracy		Ideal external resistor and capacitor		-10		+10	%
DIM Comparator Offset Voltage	V_{DIMOFS}	Voltages referred to INN			0.2		V
DIM Comparator for 100% Duty Cycle				3.3			V
PWM Duty Cycle Accuracy		V_{PWMDIM} - V_{INN} = 0.9V		23.5	25	26.5	%
		V_{PWMDIM} - V_{INN} = 2.3V		72	75	78	
PWMDIM Logic-Level Low	V_{PWMDIM_H}					0.4	V
PWMDIM Logic-Level High	V_{PWMDIM_L}			2.0			V
ANALOG DIMMING (REFI)/INTERNAL SENSE							
Current Regulation		Buck mode 8.5V < V_{INP} - V_{PGND} < 33V	R_{REFI} = 4.59kΩ (Note 3) (Note 4)	2.75	2.85	2.95	A
		Buck mode 8.5V < V_{INP} - V_{PGND} < 33V	R_{REFI} = 8.76kΩ (Note 3)	1.4325	1.5	1.5675	
			R_{REFI} = 21.8kΩ, T_J = 0°C to +125°C (Note 3)	0.564	0.6	0.636	
		Buck mode 8.5V < V_{INP} - V_{PGND} < 33V	R_{REFI} = 21.8kΩ, T_J = -40°C to +125°C (Note 3)	0.550	0.6	0.650	

Electrical Characteristics (continued)

(INP = 12V, INN = AGND = PGND, PWMDIM = INN, Limits are 100% tested at T_A = 25°C and T_A = 125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization from T_A = -40°C to T_A = 125°C.)

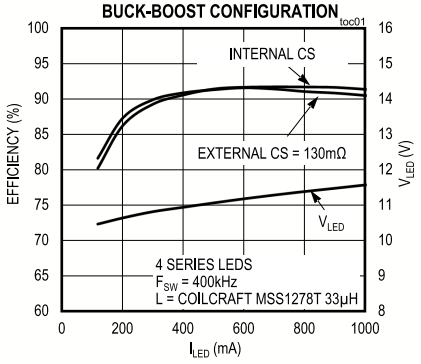
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG DIMMING (REFI)/EXTERNAL SENSE							
Current-Sense Regulation Voltage (External Sense Resistor)		FB connected to external sense resistor to AGND	V_{REFI} = 0.4V, 8.5V < V_{INP} - V_{PGND} < 31V	28.1	30	31.8	mV
			V_{REFI} = 1.2V, 8.5V < V_{INP} - V_{PGND} < 31V	0.147	0.15	0.153	V
Input Bias Current	$REFI_{IN}$	V_{REFI} = 0V to V_{CC}			20		nA
REFI Zero-Voltage Threshold	$REFI_{ZC}$	Rising threshold		0.165	0.18	0.195	V
REFI Clamp Voltage	$REFI_{CL}$			1.273	1.3	1.328	V
CONTROL LOOP							
Error Amplifier Transconductance	g_M			1.2	1.8	2.4	mS
Slope Compensation	SlopeC	Buck mode, MAX25610A		0.142	0.163	0.175	V/µs
OUT PIN							
Short Threshold	$SHRT_R$	OUT rising		140	170	200	mV
	$SHRT_F$	OUT falling		120	150	180	
Overvoltage Threshold	OV_R	OUT rising		2.85	3	3.15	V
	OV_F	OUT falling		2.75	2.9	3.05	
OUT Leakage	OUT_{LKG}					100	nA
FAULT FLAG							
Output Voltage Low	$V_{OL_\overline{FLT}}$	Referred to INN	I_{LOAD} = 5mA			200	mV
Fault Leakage Current	$\overline{FLT}_{LKG}$	Referred to INN	$V_{\overline{FLT}}$ = 5V			1	µA
Thermal Shutdown Threshold	$T_{SHUTDOWN}$	Temperature rising			165		°C
Thermal Shutdown Hysteresis	T_{HYS}				10		°C

Note 1: Bondwires are not tested in production. Estimated maximum bondwire resistance is 20mΩ.
Note 2: Extrapolated from ATE measurements at 1.9A and 0.5A.
Note 3: DC accuracy measured on ATE.
Note 4: Extrapolated from ATE measurements at 1A and 0.6A.

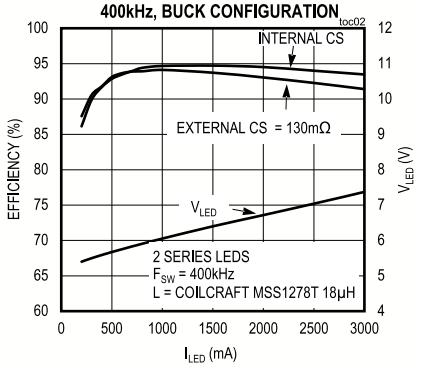
Typical Operating Characteristics

(V_{INP} = 13.5V, PWMDIM = V_{EE}, T_A = +25°C, unless otherwise noted.)

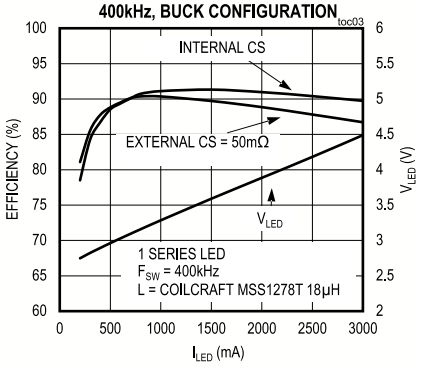
EFFICIENCY vs. LED CURRENT
BUCK-BOOST CONFIGURATION toc01



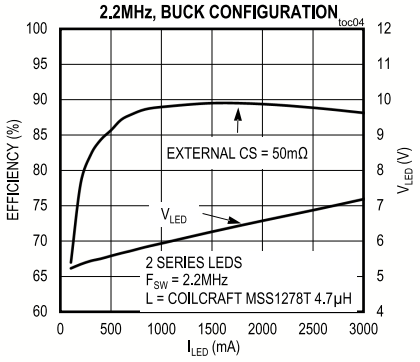
EFFICIENCY vs. LED CURRENT
400kHz, BUCK CONFIGURATION toc02



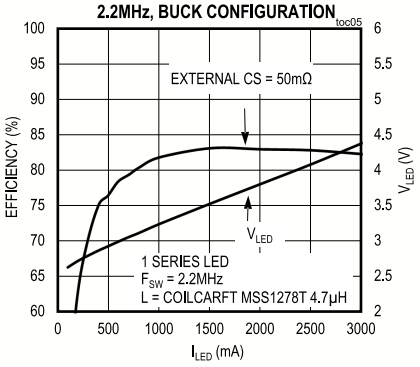
EFFICIENCY vs. LED CURRENT
400kHz, BUCK CONFIGURATION toc03



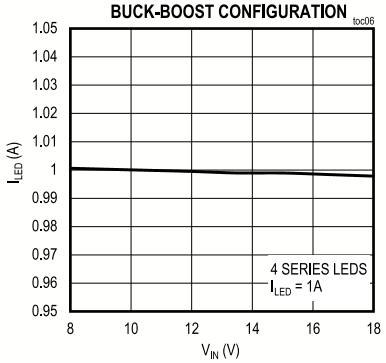
EFFICIENCY vs. LED CURRENT
2.2MHz, BUCK CONFIGURATION toc04



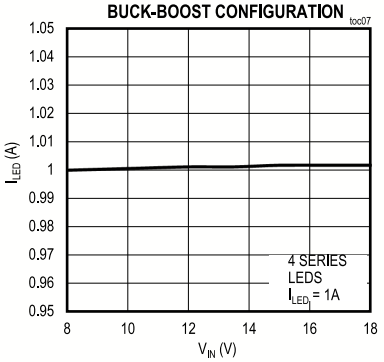
EFFICIENCY vs. LED CURRENT
2.2MHz, BUCK CONFIGURATION toc05



LINE REGULATION
EXTERNAL CURRENT SENSE
BUCK-BOOST CONFIGURATION toc06



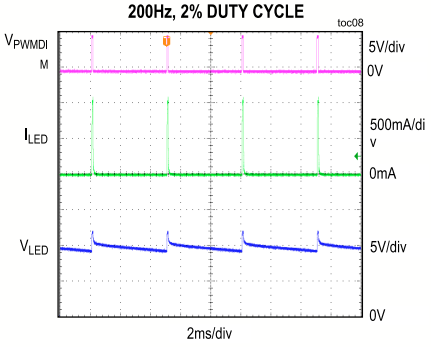
LINE REGULATION
INTERNAL CURRENT SENSE
BUCK-BOOST CONFIGURATION toc07



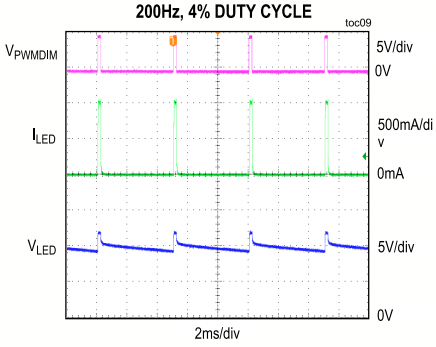
Typical Operating Characteristics (continued)

(V_{INP} = 13.5V, PWMDIM = V_{EE}, T_A = +25°C, unless otherwise noted.)

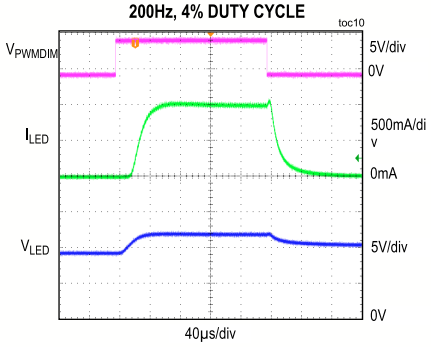
DIGITAL PWM DIMMING
200Hz, 2% DUTY CYCLE



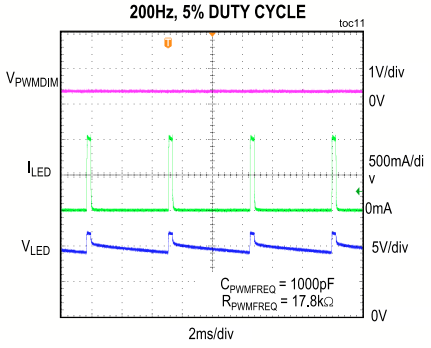
DIGITAL PWM DIMMING
200Hz, 4% DUTY CYCLE



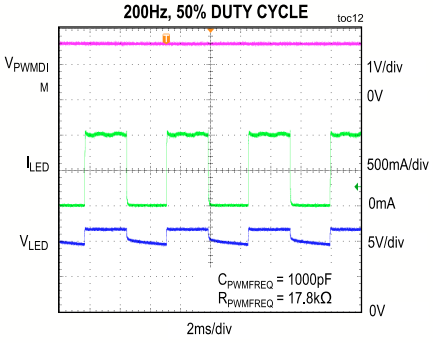
DIGITAL PWM DIMMING
200Hz, 4% DUTY CYCLE



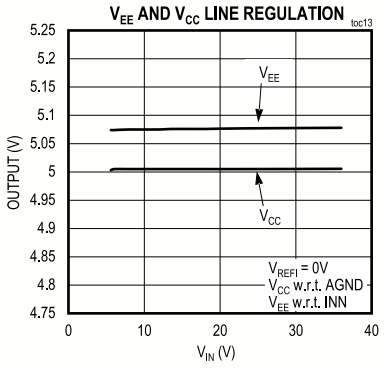
ANALOG PWM DIMMING
200Hz, 5% DUTY CYCLE



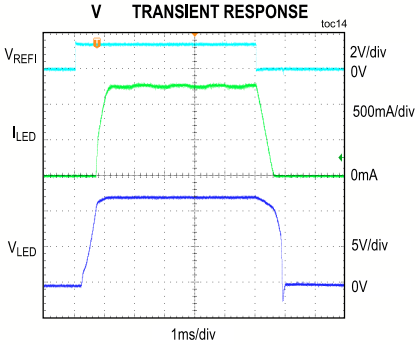
ANALOG PWM DIMMING
200Hz, 50% DUTY CYCLE



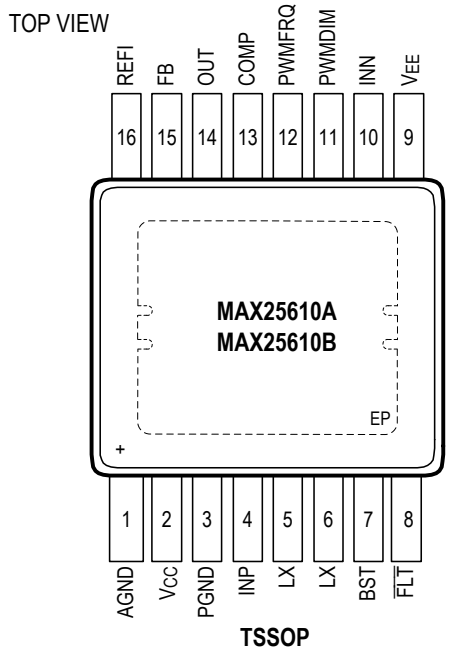
V_{EE} AND V_{CC} LINE REGULATION



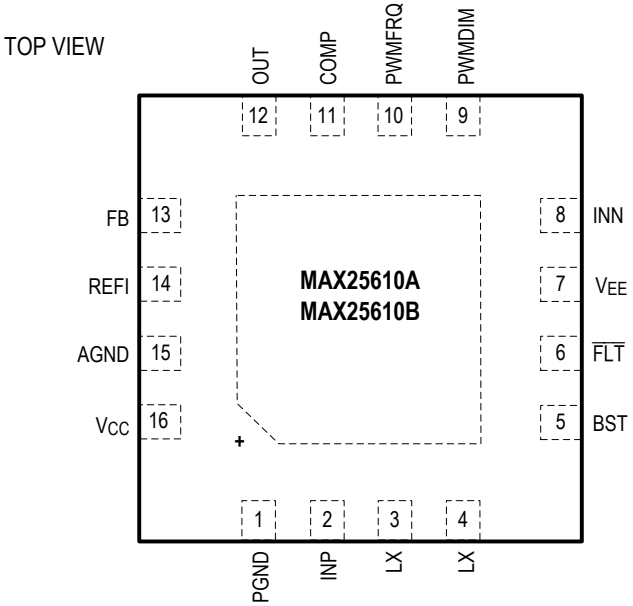
V TRANSIENT RESPONSE



Pin Configurations



TSSOP



TQFN
5mm x 5mm

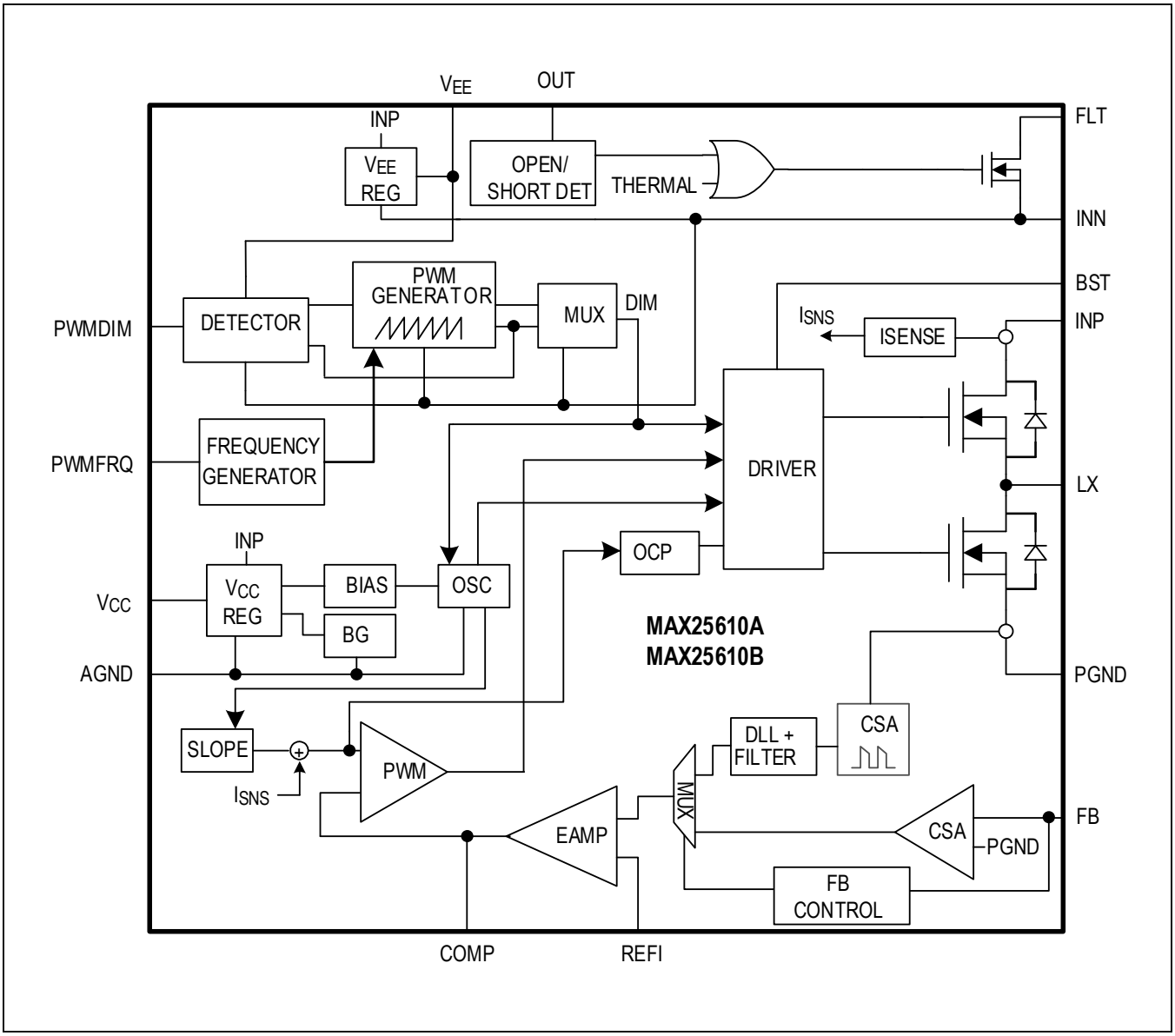
Pin Description

PIN		NAME	FUNCTION	REF SUPPLY
TSSOP	TQFN			
1	15	AGND	Analog Ground. Connect control loop compensation and other small-signal components to this ground. Connect to PGND at a single point.	
2	16	V_{CC}	Main 5V Internal LDO. Bypass this pin to AGND with a minimum 0.1µF ceramic capacitor. Bypass this pin to PGND with a minimum 1µF ceramic capacitor.	
3	1	PGND	Power Ground Reference Node. PGND is connected internally to the source terminal of internal low-side power MOSFET.	
4	2	INP	Input Positive Supply. INP is internally connected to the drain terminal of high-side power FET. Bypass this pin to PGND with a ceramic capacitor close to the pin.	
5, 6	3, 4	LX	Switching Node. Connect the output inductor to these pins with wide traces. Place the inductor as close as possible to the pins.	
7	5	BST	High-Side Power Supply for High-Side Gate Drive. Place a 0.1µF ceramic capacitor from this pin to LX.	
8	6	$\overline{FLT}$	Active-Low, Open-Drain Fault Indicator Output. Connect through an external pullup resistor to an external supply with the desired level. This pin can be left open if it is not used. See the [[Fault Handling]] section for more information.	
9	7	V_{EE}	Auxiliary 5V Regulator. Bypass this pin to INN with a minimum 1µF ceramic capacitor.	
10	8	INN	Ground Side of Input Supply. Connect this pin to PGND when used as a buck converter.	
11	9	PWMDIM	Dimming Control Input. Connect PWMDIM to an external PWM signal for PWM dimming. For analog voltage-controlled PWM dimming, connect PWMDIM to a resistive voltage-divider from V_{EE} to INN. The duty cycle is given by $D = \frac{(V_{PWMDIM} - 0.205)}{2.8}$. Connect PWMDIM to INN to turn off the LEDs. Connect PWMDIM to V_{EE} for 100% duty cycle.	
12	10	PWMFRQ	Frequency Programming for PWM Dimming Function. Connect PWMFRQ to the junction of an RC from V_{CC} to AGND. Dimming frequency is given by $f_{DIM} = \frac{3.33 \times 10^{-3}}{R_{PWMFRQ} \times C_{PWMFRQ}}$. Do not connect any other component or device to this pin.	V_{CC}

Pin Description (continued)

PIN		NAME	FUNCTION	REF SUPPLY
TSSOP	TQFN			
13	11	COMP	Compensation Network Connection. For proper compensation, connect a suitable RC network from COMP to AGND and a capacitor from COMP to AGND.	
14	12	OUT	Overvoltage Sense. Connect OUT to a resistor divider from LED+ to AGND. The typical overvoltage threshold is 3V.	
15	13	FB	LED Current-Sense Input. Connect FB to external LED current-sense resistor for external sense of LED current. Connect FB to V_{CC} through a 100kΩ resistor to enable internal current-sense regulation.	
16	14	REFI	Analog Dimming Control Input. In external current-sense mode, the voltage at REFI sets the LED current level when V_{REFI} < 1.25V. This voltage reference can be set using a resistive divider from the V_{CC} output. For V_{REFI} > 1.25V an internal reference sets the LED current. The LED current with external current sense is given by $I_{LED} = \frac{(V_{REFI} - 0.2)}{6.67R_{LED}}$. In internal current-sense mode, a resistor connected between REFI and AGND sets the current regulation. The LED current is given by $I_{LED} = \frac{13125}{R_{REFI}}$.	

Functional Diagrams



Detailed Description

The MAX25610A/MAX25610B are fully synchronous LED drivers that provide constant output current to drive high-power LEDs. The MAX25610A/MAX25610B integrate two 60mΩ power MOSFETs for synchronous operation, minimizing external components. Flexible configuration supports buck, inverting buck-boost and boost conversion. The device incorporates current-mode control that provides fast transient response and eases loop stabilization. The MAX25610A/MAX25610B include cycle by cycle current limiting, output overvoltage protection (OVP), open-string protection, output short-circuit protection (SCP), and thermal shutdown.

In LED driver applications, the MAX25610A/MAX25610B provide analog dimming of the LED current through the REFI pin and PWM dimming through the PWMDIM pin. Switching is enabled when PWMDIM is high and disabled with both MOSFETs off when PWMDIM is low. Analog programming of the PWMDIM pin enables the built-in digital dimming function, with dimming frequency selected by the PWMFRQ pin.

The MAX25610A/MAX25610B include two 5V regulators. A regulated 5V between V_{CC} and AGND is used for IC bias, as well as REFI and PWMFRQ programming. Another low current regulated 5V between V_{EE} and INN is used for analog PWMDIM and $\overline{FLT}$ pullup. Both PWMDIM and $\overline{FLT}$ reference INN for easy system interface. Switching frequency is internally set at 400kHz for the MAX25610A and 2.2MHz for the MAX25610B. The devices have built-in spread spectrum to reduce EMI noise. External and internal current sense are supported, with ±3% and ±6% respective LED current accuracy.

The MAX25610A/MAX25610B are well-suited for automotive applications that require high-voltage input and can withstand load dump events up to 40V. The devices can also be used as DC-DC converters using the FB input as feedback for the output voltage divider. The MAX25610A/MAX25610B are available in thermally enhanced 16-pin TSSOP-EP and 16-pin TQFN packages. They are specified to operate over the -40°C to +125°C automotive temperature range.

Functional Operation

The MAX25160A/MAX25610B are fully synchronous, monolithic, constant frequency peak current-mode DC-DC LED drivers. These devices support both internal and external current sensing of the LED current. Upon power-up, the device detects the voltage level of the FB pin to determine the current sense configuration. External LED current sensing is configured by connecting the FB pin to an external sense resistor in series with LED string. The devices regulate the current to the programmed voltage at the REFI pin. Internal LED current sensing is selected by connecting the FB pin to V_{CC} through a 100kΩ resistor. The devices use an integrated current sense of the low-side power FET and regulate that current to the programmed current at the REFI pin.

The fixed-frequency oscillator turns on the internal high-side power FET at the beginning of each clock cycle. Current in the inductor then increases until the internal PWM comparator trips and turns off the high-side power FET. When the high-side power FET turns off, the synchronous low-side power FET turns on until the next clock cycle begins.

In external LED current sensing, the FB voltage is amplified by a factor of 6.67 and fed to the inverting input of a transconductance amplifier, while the REFI voltage is fed to the noninverting input. In internal current sensing, the transconductance amplifier compares the current programmed at REFI against the current sensed across the low-side power FET. In both cases, the error signal at the inputs of the transconductance amplifier generate a proportional current out the COMP pin. COMP is externally compensated by a resistor and capacitor network. The compensated COMP voltage is fed to the noninverting input of a PWM comparator. The inverting input of the PWM comparator is a signal that represents the current on the high-side power FET summed with a saw-toothed ramp.

The devices also include a PWMDIM dimming input that is used for PWM dimming of the LED current. When this signal is low, both the high-side and low-side power FETs are turned off. When the PWMDIM signal goes high the LED current regulation starts. The rising edge of the PWMDIM signal also restarts the internal oscillator to allow the high-side power FET to be turned on at the same time as the rising edge of the PWMDIM signal. This provides consistent dimming performance at low dimming duty cycles. Analog programming of the PWMDIM pin operates in the same way as described above, except that it uses an internal PWM clock with dimming frequency selected by the PWMFRQ pin.

Mode Selection

The devices can operate in two modes. Connect a 2.49kΩ resistor from V_{CC} to PWMFRQ pin for operation in buck mode. Connect a 17.8kΩ resistor from V_{CC} to PWMFRQ pin to operate in buck-boost or boost mode.

LED Current Sense

The device can use both internal and external current sense for the LED current. For external LED current sense a resistor is connected between the cathode of the last LED in the string and ground. The FB pin is connected to the cathode of the LED string. The regulated LED current is given by:

$$I_{LED} = \frac{(V_{REFI} - 0.2)}{6.67R_{LED}}$$

where:

V_{REFI} is in volts,

R_{LED} is in ohms.

For internal current sense, connect FB pin to V_{CC} with a 100kΩ resistor. The LED current is now sensed by the current flowing in the bottom MOSFET. When using internal current sense, the REFI pin should only have a resistor to AGND. The LED current is then given by:

$$I_{LED} = \frac{13125}{R_{REFI}}$$

Analog Dimming

The device has an analog dimming control input pin (REFI). In external sensing mode, the voltage at REFI sets the LED current level when REFI ≤ 1.2V. For higher voltages, REFI is clamped to 1.25V (typ). The LED current is guaranteed to be at zero when the REFI voltage is at or below 0.18V (typ). The LED current can be linearly adjusted from zero to full scale for REFI voltages in the range of 0.2V to 1.2V.

In internal sensing an external resistor from REFI pin to ground is used to program the LED current. The REFI pin voltage is regulated to 1.25V in this mode. The LED current is then given by:

$$I_{LED} = \frac{13125}{R_{REFI}}$$

V_{CC} Regulator

The devices feature a 5V linear regulator (V_{CC}) that is powered by the input voltage on INP. The V_{CC} regulator provides power to all the internal logic, control circuitry, and the gate drivers. Bypass V_{CC} to AGND with a minimum of 0.1µF ceramic capacitor as close as possible to the devices. Bypass V_{CC} to PGND with a minimum of 1µF ceramic capacitor as close as possible to the device.

V_{EE} Regulator

The devices include a 5V V_{EE} regulator that generates a 5V supply referenced to INN. This regulator powers the internal PWM dimming and fault indication circuitry. This regulator can provide a maximum of 2mA to external circuits. Bypass V_{EE} to INN with a minimum 1µF ceramic capacitor as close as possible to the devices. The V_{EE} regulator features an output UVLO that stops switching of the MAX25610A/MAX25610B when the V_{EE} voltage goes below the typical UVLO threshold of 4.25V.

BST Supply

The BST pin provides the drive voltage to the high-side switching MOSFET. Connect a 0.1µF ceramic capacitor from this pin to the LX pin. Place the capacitor as close as possible to BST pin. The BST capacitor is charged from an internal diode from V_{CC} when LX goes low.

Input UVLO

The devices have an integrated UVLO that disables switching when the voltage from INP to INN falls below an internal threshold. When the device is set for operation in the buck-boost mode switching is enabled when the input voltage exceeds 4.5V(typ) and disabled when the voltage drops below 4V (typ). If the device is set for operation in the buck mode, the switching is enabled when the voltage exceeds 8.0V (typ) and is disabled when the voltage drops below 7.75V (typ).

Cycle-by-Cycle Current Limit

The MAX25610A/MAX25610B implement a cycle-by-cycle current limit on the internal high-side power switch. If the peak current in the high-side switch exceeds 4.25A (typ), the switch is turned off immediately. The high-side switch turns on again at the start of the next clock cycle.

Slope Compensation

The devices incorporate slope compensation to prevent sub-harmonic oscillations for duty cycles exceeding 50%. When the device is configured for buck mode the slope compensation ramp rate is 562mA/µs for the MAX25610A and 2.9A/µs for the MAX25610B. When configured as a buck-boost converter, the slope compensation ramp is proportional to the output voltage. The slope compensation ramp rate for the buck-boost converter is (slope = $0.078V_{OUT}$)A/µs in the MAX25610A.

Spread Spectrum

The devices use a triangular spread-spectrum modulation technique to reduce the EMI for frequencies less than 30MHz. The spread spectrum is internally set at +6%. The switching frequency increases linearly from a low of 0.94 times the programmed frequency to a high of 1.06 times the programmed frequency. The modulation frequency of the triangular pattern is 0.2% of the programmed switching frequency. For the MAX25610A, the modulation frequency is 800Hz. For the MAX25610B, the modulation frequency is 4.5kHz.

Overvoltage Protection

If the voltage from INP to PGND exceeds 34.5V (typ) in the buck-boost and boost configuration, the LED current regulation is disabled and both the internal MOSFETs are turned off. Switching is enabled once the voltage from INP to PGND goes below 33.3V (typ). In the buck mode, the devices keep switching at all input voltages above input UVLO.

Error Amplifier

An internal transconductance amplifier with a transconductance of 1800µS is used by the control loop in the MAX25610A/MAX25610B to regulate the LED current. In external LED current sensing, the FB voltage is amplified by a factor of 6.7 and fed to the inverting input of a transconductance amplifier, while the REFI voltage is fed to the noninverting input. In internal current sensing, the transconductance amplifier compares the current programmed at REFI against the current sensed across the low-side power FET. In both cases, the error signal at the inputs of the transconductance amplifier generate a proportional current out the COMP pin. COMP is externally compensated by a resistor and capacitor network. The compensated COMP voltage is fed to the non-inverting input of a PWM comparator. The inverting input of the PWM comparator is a signal that represents the current on the high-side power FET summed with a with a slope compensation ramp.

When the PWM dimming signal is low the COMP pin is internally disconnected from the output of the error amplifier. When the dimming signal is high, the output of the error amplifier is connected to COMP. This enables the compensation capacitor to hold the charge when the dimming signal has turned off the internal switching MOSFETs. To maintain the charge on the compensation capacitor C_{COMP}, the capacitor should be a low-leakage ceramic type. When the internal dimming signal is enabled, the voltage on the compensation capacitor forces the converter into steady state almost instantaneously.

PWM Dimming

The PWMDIM pin is used to enable/disable the internal switching MOSFETs, and also for pulse width modulated dimming. When PWMDIM is high (> $2V_{MIN}$), the devices enable the internal oscillator, and MOSFET switching resumes. This synchronizes operation and eliminates flicker during low pulse widths. When PWMDIM is low (< $0.4V_{MAX}$), current regulation is stopped. Both internal MOSFETS are three-stated, and the output of the error amplifier is disconnected from the external components on the COMP pin.

The PWMDIM pin is also used for PWM dimming in two modes, one programmed with an analog voltage, and the other using a digital signal.

Internal PWM Dimming Frequency Generator

An internal PWM frequency generator is implemented with an RC connected at the PWMFRQ pin. The resistor R_{PWMFRQ} is connected from PWMFRQ to V_{CC} and a capacitor C_{PWMFRQ} is connected from PWMFRQ to AGND. R_{PWMFRQ} needs to be 2.49kΩ when the device is used in buck mode and 17.8kΩ when used in buck-boost or boost mode. The ceramic capacitor from PWFRQ to AGND should be in the range of 300pF to 6.8nF. It is recommended to use ceramic capacitors with low tolerances for accurate frequency programming. COG and NPO dielectrics are preferred.

The internal PWM dimming frequency is given by:

$$f_{DIM} = \frac{3.33 \times 10^{-3}}{R_{PWMFRQ} \times C_{PWMFRQ}}$$

Table 1 lists some examples for the dimming frequency.

For external digital PWM dimming use a minimum capacitance of 220nF for C_{PWMFRQ}.

Analog Mode PWM Dimming

If an analog control signal is applied to PWMDIM, the device compares the DC input to an internally generated ramp to pulse-width-modulate the LED current. The ramp frequency is set by an RC network on the PWMFRQ pin. The output-current duty cycle is linearly adjustable from 0% to 100% (0.2V < V_{PWMDIM} < 3V). The PWM dimming duty cycle in analog mode is given by:

$$D = \frac{(V_{PWMDIM} - 0.205)}{2.8}$$

where V_{PWMDIM} is the voltage applied to PWMDIM in volts.

Table 1. PWMDIM Frequency Selection

MODE	RPWMFRQ (KΩ)	CPWMFRQ	PWMDIM FREQUENCY (HZ)
Buck	2.49	1.2nF	1114
		2.7nF	495
		3.3nF	405
		4.3nF	311
		6.8nF	197
Buck-Boost or Boost	17.8	300pF	624
		360pF	520
		470pF	398
		620pF	302
		910pF	206

Digital Mode PWM Dimming

If a TTL-level digital input signal is applied to PWMDIM pin, the duty cycle determines the dimming ratio and the frequency is set by the digital input pulse frequency.

Thermal Protection

The devices feature thermal protection. When the junction temperature exceeds +165°C, the internal MOSFETs stop switching resulting in the reduction in power dissipation in the device. The part returns to regulation once the junction temperature falls below +155°C. Both the V_{CC} and V_{EE} regulators continue to regulate even during thermal shutdown.

Fault Flag

Fault Behavior External Sensing

LED Short Fault

During external current sensing, the devices can detect a short between the anode and the cathode of the LEDs. The following conditions need to be satisfied simultaneously to detect and flag an LED short fault:

1) OUT voltage < SHRT threshold (150mV, typ)
2) End of startup blanking timer (650µs, typ)

The startup timer is cumulative during dimming high phases; the timer is suspended during dimming low phases. The total cumulative on duration of successive dimming pulses should exceed 650µs to activate fault detection.

Once an LED short is detected, the $\overline{FLT}$ flag asserts low.

Short-to-PGND Fault

During external current sensing, the devices can detect a short between the anode of the LED string and the ground terminal. The following conditions need to be satisfied at the same time to detect and flag a PGND short fault:

1) OUT voltage < SHRT threshold (150mV, typ)
2) COMP > 3.4V (typ)
3) End of startup blanking timer (650µs, typ)

Once an LED PGND short is detected, $\overline{FLT}$ is asserted low, the current regulation is stopped, and the internal power MOSFETs switch off. This latch-off condition persists until power is recycled.

LED Open Fault

The devices can detect an open circuit on the LED string. The following condition needs to be satisfied simultaneously to detect and flag an LED open fault:

1) OUT voltage > OV threshold (typ 3V)

Once an LED open is detected, $\overline{FLT}$ is asserted low, the current regulation is stopped, and the internal MOSFETs go into a high-impedance state. This latch-off condition persists until the OUT pin voltage drops below 2.9V (typ).

Fault Behavior Internal Sensing

LED Short Fault

During internal current sensing, the devices can detect a short between the anode and the cathode of LED string or between anode of the LED string and PGND. The following conditions need to be satisfied simultaneously to detect and flag a SHORT fault:

1) OUT voltage < SHRT threshold (150mV, typ)
2) REFI resistor < 280kΩ (typ)
3) End of startup blanking timer (650µs, typ)

Once an LED short is detected, the $\overline{FLT}$ flag is asserted low. The current continues to be regulated even if the short is between LED+ and LED- or between LED+ and PGND.

LED Open Fault

During Internal current sensing, the devices can detect an open circuit in the LED string. The following conditions need to be satisfied simultaneously to detect and flag a LED-OPEN fault:

1) OUT voltage > OV threshold (3V, typ)

Once LED open is detected, $\overline{FLT}$ is asserted low, the current regulation is stopped, and the internal MOSFETs go into a high-impedance state. This latch-off condition persists until the OUT pin voltage drops below 2.9V (typ).

V_{EE} UVLO Fault

The devices also feature an V_{EE} undervoltage lockout fault. When the V_{EE} voltage goes below its UVLO level of 4.25V (typ), the fault flag $\overline{FLT}$ asserts low.

Thermal Shutdown Fault

The $\overline{FLT}$ pin goes low when thermal shutdown is activated.

Exposed Pad

The device package features an exposed thermal pad on its underside to use as a heat sink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PCB. Connect the exposed pad and AGND together using a large pad or ground plane, or multiple vias to the AGND plane layer.

Applications Information

Inductor

The peak inductor current and the allowable inductor current ripple determine the value and size of the output inductor.

In the buck LED driver, the average inductor current is the same as the LED current. The peak inductor current occurs at the maximum input line voltage where the duty cycle is at the minimum:

$$D_{MIN} = \frac{V_{LED}}{V_{INMAX}}$$

where:

V_{LED} is the forward voltage of the LED string

V_{INMAX} is the maximum input supply voltage

The maximum peak-to-peak inductor ripple (ΔIL) occurs at the maximum input line. The peak inductor current is given by:

$IL_{PK} = I_{LED} + 0.5 \times \Delta IL$

The inductance value of inductor L_{BUCK} is calculated as:

$$L_{BUCK} = \frac{V_{INMIN} \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where:

f_{SW} is the switching frequency.

For the MAX25610A, f_{SW} is 400kHz and for the MAX25610B f_{SW} is 2.2MHz. Choose an inductor that has a minimum inductance greater than the calculated value.

Boost and buck-boost configurations are similar in that the total output voltage seen by the inductor is always higher than the input voltage. The difference being that, for the boost configuration, the total output voltage is dependent on the total LED voltage, while for the buck-boost configuration, the total output voltage is dependent on the sum of the LED voltage and the input voltage.

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage.

For the boost converter, the average inductor current is equal to the input current. Calculate the maximum duty cycle using the following equation:

$$D_{MAX} = \frac{(V_{LED} - V_{INMIN})}{V_{LED}}$$

where:

V_{LED} is the forward voltage of the LED string

V_{INMIN} is the minimum input supply voltage

Actual voltages for the above can be determined once component selection is completed.

In the buck-boost LED driver, the average inductor current is equal to the input current plus the LED current. Calculate the maximum duty cycle using the following equation:

$$D_{MAX} = \frac{V_{LED}}{(V_{LED} + V_{INMIN})}$$

with the variables being the same as defined in the calculation of the boost configuration.

For both boost and buck-boost configurations, use the following equations to calculate the maximum average inductor current (IL_{DC_MAX}), peak-to-peak inductor current ripple (ΔIL), and the peak inductor current (IL_{PK}) in amperes:

$IL_{DC_MAX} = I_{LED}/(1 - D_{MAX})$

Allowing the peak-to-peak inductor ripple to be ΔIL, the peak inductor current is given by:

$IL_{PK} = IL_{DC_MAX} + 0.5 \times \Delta IL$

The inductance value of inductor L_{BOOST} or $L_{BUCK-BOOST}$ is calculated as:

$$L = \frac{V_{INMIN} \times D_{MAX}}{f_{SW} \times \Delta IL}$$

where f_{SW} is the switching frequency, V_{INMIN} and ΔIL are defined above. Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than IL_{PK} at the operating temperature.

To avoid sub-harmonic oscillation in the current-mode controlled regulators when duty cycle is greater than 50%, the inductor value should be set to match the slope compensation value at the designed frequency. The selected inductor should satisfy the following condition.

$$\frac{2 \times V_{OUT}}{SLOPE} > L > \frac{V_{OUT}}{2 \times SLOPE}$$

Input Capacitor

The input-filter capacitor bypasses the ripple current drawn by the converter and reduces the amplitude of high-frequency current conducted to the input supply. The ESR, ESL, and bulk capacitance of the input capacitor contribute to the input ripple. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current from the converter. The input capacitors must also be chosen such that the capacitors can withstand the maximum expected input voltage with adequate design margin.

In the buck configuration, the minimum value of the input capacitance is given by:

$$C_{MIN} > \frac{I_{LED}}{4 \times \eta \times f_{SW} \times \triangle V_{IN}}$$

where:

I_{LED} is the maximum LED current

η is the efficiency

f_{SW} is the switching frequency

ΔV_{IN} is the acceptable input voltage ripple

For the buck-boost configuration, the minimum value of the input capacitance is given by:

$$C_{MIN} > \frac{I_{LED} \times D_{MAX}}{\eta \times f_{SW} \times \triangle V_{IN}}$$

where:

D_{MAX} is the maximum duty cycle that occurs at low line

In the boost configuration, the minimum value of the input capacitance is given by:

$$C_{MIN} > \frac{\triangle I_L}{4 \times f_{SW} \times \triangle V_{IN}}$$

where:

ΔI_L is the peak to peak inductor ripple at low line.

Note that the DC bias on the capacitor can derate the capacitance value. The capacitance value can also change due to temperature. The selected capacitor should have a capacitance that exceeds the minimum required capacitance at the maximum operating voltage and maximum operating temperature.

Output Capacitor

With adequate design margin, the output capacitors can withstand the maximum operating output voltage. The output voltage ripple (ΔV_{OUT}) is a function of the output capacitance, its ESR, and ESL. Ceramic output capacitors have very low ESR and ESL so the output ripple in ceramic capacitors are purely a function of the ripple current and the capacitance.

In the case of the buck converter, the minimum value of the output capacitance is given by:

$$C_{MIN} > \frac{\triangle I_L}{8 \times f_{SW} \times \triangle V_{OUT}}$$

where:

ΔI_L is the peak to peak output ripple at the maximum input voltage

ΔV_{OUT} is the maximum allowable output ripple

In the case of the buck-boost converter, the minimum value of the output capacitance is given by:

$$C_{MIN} > \frac{I_{LED} \times V_{OUT}}{(V_{INMIN} + V_{OUT}) \times f_{SW} \times \triangle V_{OUT}}$$

where:

V_{INMIN} is the minimum input voltage

In the case of the boost converter, the minimum value of the output capacitance is given by:

$$C_{MIN} > \frac{I_{LED} \times V_{OUT}}{(V_{INMIN} + V_{OUT}) \times f_{SW} \times \triangle V_{OUT}}$$

Compensation

Table 2 shows suggested values of inductor, Output capacitor and compensation components for the buck and buck-boost configurations.

Buck External Sense

The loop gain equation is given by:

$$(f) = GM \times Z_{COMP} \times G_{CS} \times Z_{OUT} \times \left(\frac{R_{SENSE}}{R_{SENSE} + R_{LED}}\right) \times 6.67$$

Where:

GM is the transconductance of error amplifier = 1.8mS

G_{CS} is transconductance from comp pin to peak inductor current = 3.33

Z_{COMP} is the impedance of R_{COMP} in series with C_{COMP}

R_{LED} is the dynamic resistance of LED

Z_{OUT} is the output impedance which is the parallel impedance of R_{SENSE} + R_{LED} with C_{OUT}

Choose:

$$R_{COMP} = \frac{1}{2\pi \times F_P \times C_{COMP}}$$

$$Fp = \frac{1}{2\pi\left(R_{SENSE} + R_{LED}\right) \times C_{OUT}}$$

$$C_{COMP} = G_{CS} \times G_M \times R_{SENSE} \times \frac{6.67}{2\pi Fu}$$

Where:

F_P is the Load pole frequency

Fu is the unity gain frequency, choose Fu = 40kHz

The R_{COMP} and C_{COMP} values are given in Table 2 for a typical 1 or 2 LED application.

Buck Internal Sense

The compensation component values do not depend on the output pole. For internal sensing applications in buck mode set:

R_{COMP} = 0Ω

C_{COMP} = 100nF

Buck-Boost External Sense

Loop gain equation is given by:

$$A(f) = G_M \times Z_{COMP} \times G_{CS} \times Z_{OUT} \times \frac{V_{IN}}{V_{IN} + 2 \times V_{OUT}} \times \frac{R_{SENSE}}{R_{SENSE} + R_{LED}} \times 6.67$$

The right half plane zero for a Buck-Boost is given by:

$$F_{RHP} = \frac{V_{LED} \times (1 - D)^2}{2\pi \times I_{LED} \times L \times D^2}$$

where:

V_{LED} is the voltage across the LED string

D is the maximum duty cycleV_{IN} is the Input Voltage V_{OUT} is the LED string voltage taken positive.

The unity gain frequency is chosen 1/6th of F_{RHP}.

Choose:

$$R_{COMP} = \frac{1}{2\pi \times F_P \times C_{COMP}}$$

where:

F_P is load pole frequency

$$F_P = \frac{1}{2\pi \times \left(R_{SENSE} + R_{LED}\right) \times C_{OUT}}$$

C_{COMP} value is:

$$C_{COMP} = \frac{GM \times V_{IN} \times G_{CS} \times 6.67 \times R_{SENSE}}{2\pi \times \left(V_{IN} + 2 \times V_{OUT}\right) \times F_U}$$

F_U is the unity gain frequency

The R_{COMP} and C_{COMP} values are given in Table 2 for a typical 2 LEDs application.

Table 2. Recommended Components—Various Configurations

CONFIGURATION	PART NAME	C_{COMP} (NF)	R_{COMP} (Ω)	C_{OUT} (MF)	L_{OUT} (MH)
Buck—External Current Sense	MAX25610A	22	75	2.2	22
Buck—External Current Sense	MAX25610B	22	75	2.2	4.7
Buck—Internal Current Sense	MAX25610A	100	0	2.2	22
Buck-Boost—External Current Sense	MAX25610A	220	100	20	33
Buck-Boost—Internal Current Sense	MAX25610A	220	62	20	33

Buck-Boost Internal Sense

The compensation component values do not depend on the output pole.

$$C_{COMP} = \frac{GM}{2\pi \times F_U}$$

Where:

F_U is the unity gain frequency = 1/6th of F_{RHP}.

Choose:

$$R_{COMP} = \frac{1}{2\pi \times C_{COMP} \times 12kHz}$$

The R_{COMP} and C_{COMP} values are given in Table 2 for a typical 4 LED application.

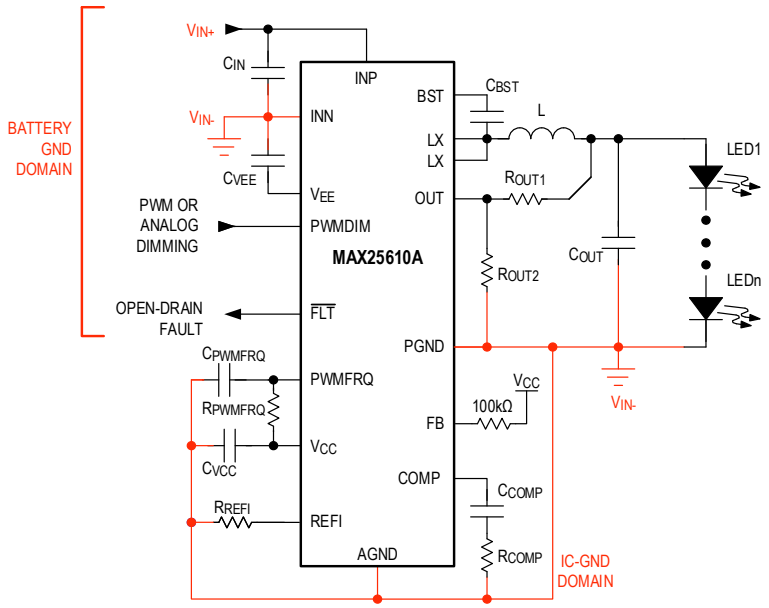
PCB Layout Guidelines

For proper operation and minimum EMI, use the following PCB layout guidelines:

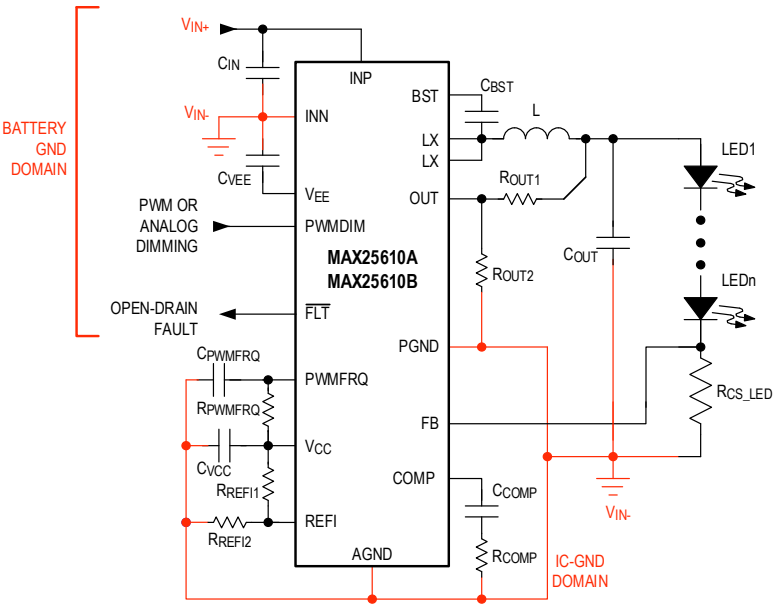
- All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small current loop areas reduce radiated EMI.
- Place a 0603 0.1µF ceramic capacitor between INP and PGND. Also place 2x 10µF ceramic capacitors as close as possible between INP and PGND. These capacitors provide the high-frequency switching currents to the internal MOSFETs and their drivers. In case of the buck-boost topology, add additional capacitance between INP and INN.
- Place a minimum 1µF ceramic bypass capacitor between V_{CC} and PGND and another minimum 0.1µF ceramic capacitor between V_{CC} and AGND.
- Place a minimum 1µF ceramic bypass capacitor between V_{EE} and INN.
- Place the BST capacitor close to the pins BST and LX.
- Place an unbroken ground plane on the layer closest to the surface layer with the inductor, device, and the input and output capacitors.
- The surface area of the LX and BST nodes should be as small as possible to minimize emissions.
- The exposed pad on the bottom of the package must be soldered to AGND of the IC so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the device to additional ground planes within the circuit board.
- Run the current-sense lines FB and the line from the bottom side of the current-sense resistor very close to each other. The Kelvin line from the bottom of the current-sense resistor when doing external current sensing should go directly to the AGND pin of the IC. Do not cross these critical signal lines with switching power lines.
- Use separate ground planes on different layers of the PCB for AGND and PGND. All the components connected to the pins REFI, COMP, OUT, and PWMFRQ go to the AGND plane. Connect both of these planes together at a single point where the switching activity is minimum.
- When using the PWMDIM pin for performing PWM dimming with a DC voltage generated using a resistive divder from the V_{EE} supply, ensure that the bottom resistor of the resistive divider is connected to the INN plane where it is quiet.
- Use 2oz or thicker copper to keep trace inductances and resistances to a minimum. Thicker copper conducts heat more effectively, thereby reducing thermal impedance. Thin copper PCBs compromise efficiency in applications involving high currents.

Typical Application Circuits

Buck LED Driver

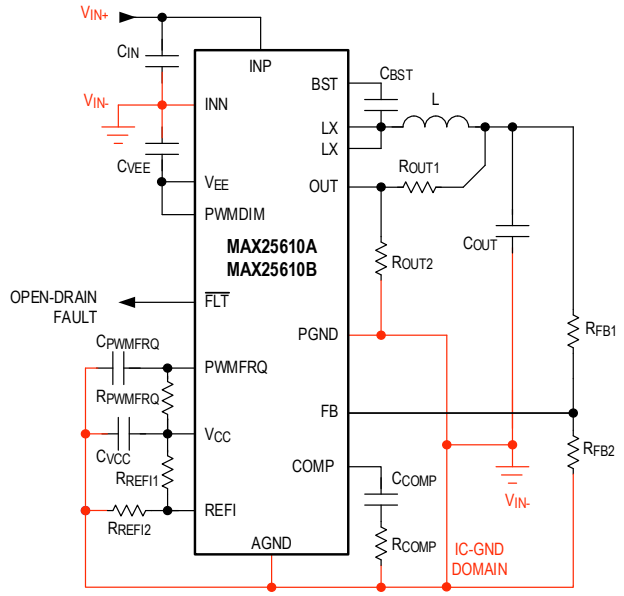


Buck LED Driver with Accurate Current Regulation

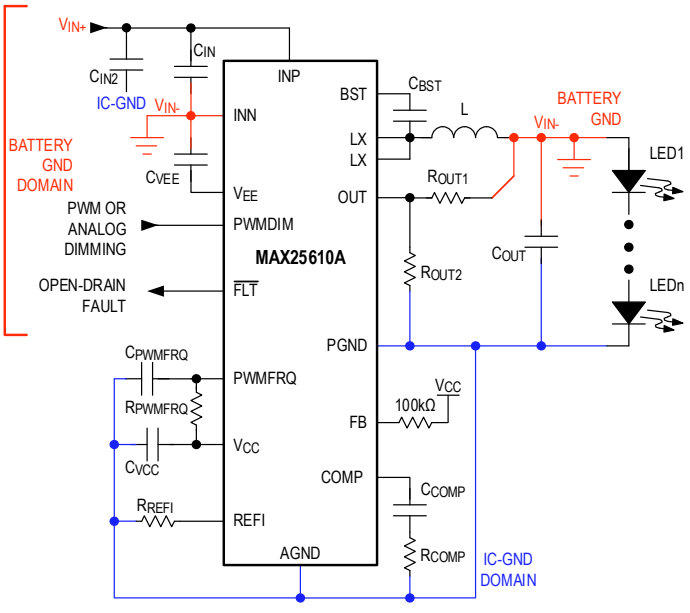


Typical Application Circuits (continued)

Buck DC-DC Converter

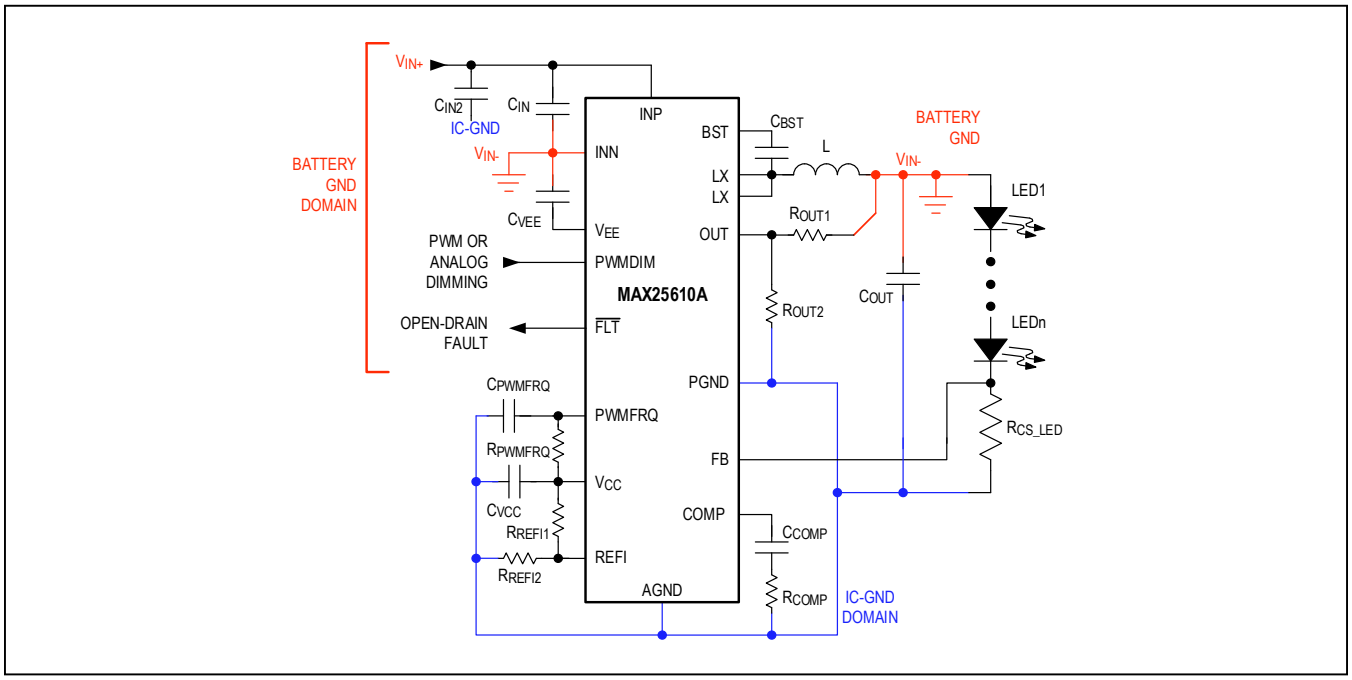


Buck Boost LED Driver

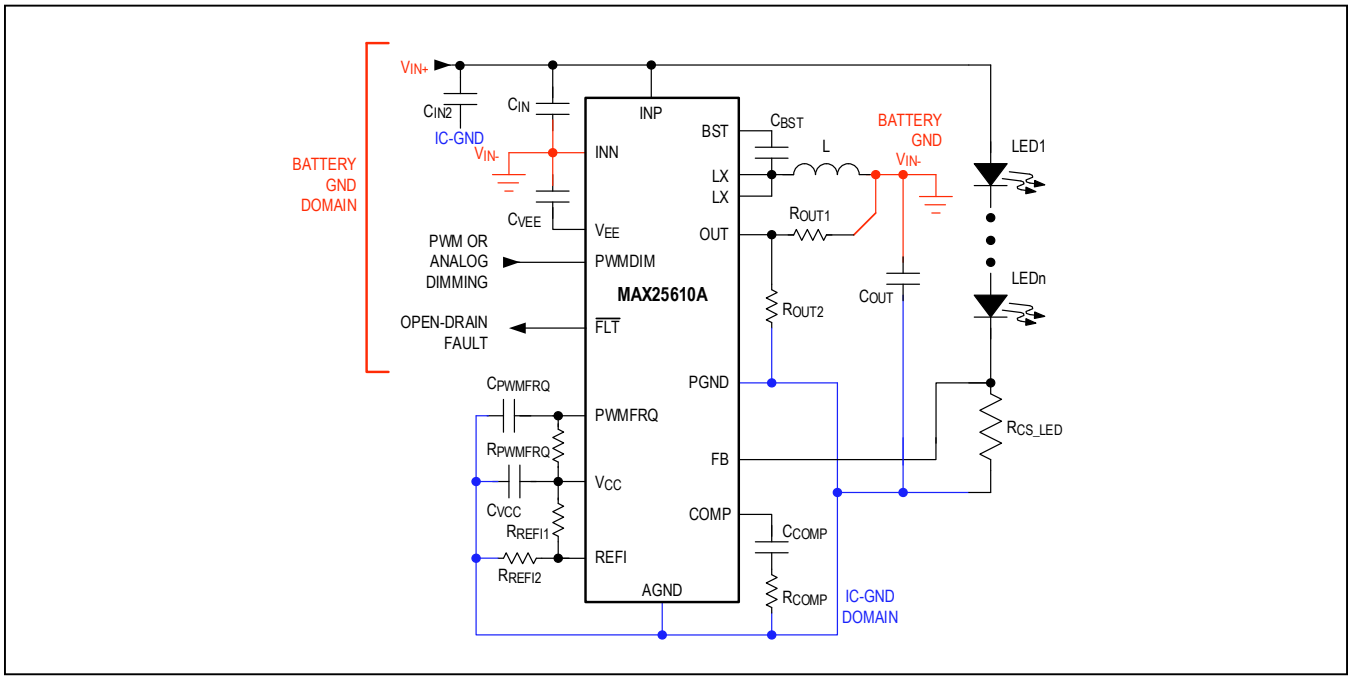


Typical Application Circuits (continued)

Buck Boost Regulator with Accurate Regulation



Boost LED Driver



Ordering Information

PART	TEMP RANGE	FREQUENCY	PIN-PACKAGE
MAX25610AAUE/V+	-40°C to +125°C	400kHz	16 TSSOP
MAX25610BAUE/V+	-40°C to +125°C	2.2MHz	16 TSSOP
MAX25610AATE/VY+	-40°C to +125°C	400kHz	16 TQFN
MAX25610BATE/VY+	-40°C to +125°C	2.2MHz	16 TQFN
MAX25610AAUE+	-40°C to +125°C	400kHz	16 TSSOP
MAX25610BAUE+	-40°C to +125°C	2.2MHz	16 TSSOP
MAX25610AATEY+	-40°C to +125°C	400kHz	16 TQFN
MAX25610BATEY+	-40°C to +125°C	2.2MHz	16 TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—
1	12/18	Updated *Electrical Characteristics*, *Ordering Information*, and equation	4, 14, 23
2	2/19	Updated PWMFRQ equation in *Pin Description*, removed future-product status from MAX25610BAUE/V+, MAX25610AATE/VY+, and MAX25610BATE/VY+, added MAX25610AAUE+*, MAX25610BAUE+*, MAX25610AATEY+*, and MAX25610BATEY+* in *Ordering Information*	9, 23
3	3/19	Added future-product status to MAX25610BAUE/V+* and MAX25610BATE/VY+* in *Ordering Information*	23
4	3/19	Delete the future-product status to MAX25610BAUE/V+ and MAX25610BATE/VY+ in *Ordering Information*	23
5	4/19	Remove future-product status from non/V parts in *Ordering Information*	23

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